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SANTA BARBARA  
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**DEVELOPMENT OF 256 x 256 ELEMENT  
IMPURITY BAND CONDUCTION  
INFRARED DETECTOR ARRAYS  
FOR ASTRONOMY**

**FINAL REPORT  
JUNE 1997**

PREPARED FOR  
NASA - AMES RESEARCH CENTER  
MOFFETT FIELD, CA 94035-1000

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Prepared For  
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Prepared By  
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## TABLE OF CONTENTS

	SECTION	PAGE
<b>1</b>	<b>EXECUTIVE SUMMARY .....</b>	<b>1</b>
1.1	Program Objective.....	1
1.2	Program Approach .....	1
1.3	Program Execution.....	2
1.4	Experimental Results.....	2
1.5	Future Activity .....	3
1.6	Cost and Schedule.....	3
<b>2</b>	<b>INITIAL DATA ANALYSIS.....</b>	<b>4</b>
<b>3</b>	<b>EPITAXIAL GROWTH.....</b>	<b>9</b>
3.1	Epitaxial Wafer Selection.....	9
3.2	Epi Growth.....	11
<b>4</b>	<b>DETECTOR FABRICATION.....</b>	<b>16</b>
4.1	Wafer Selection.....	16
4.2	Detector Wafer Processing .....	18
4.3	Back End Processing .....	18
<b>5</b>	<b>DETECTOR TEST.....</b>	<b>23</b>
5.1	Test Preparation .....	23
5.2	Detector Test Facilities .....	23
5.3	Detector Test Results.....	27
<b>6</b>	<b>READOUTS .....</b>	<b>30</b>
<b>7</b>	<b>SCA FABRICATION .....</b>	<b>33</b>
<b>8</b>	<b>SCA TEST RESULTS .....</b>	<b>34</b>
<b>9</b>	<b>CONCLUSION.....</b>	<b>37</b>
	<b>SF298 REPORT DOCUMENTATION PAGE.....</b>	<b>39</b>

## FIGURES

FIGURE	TITLE	PAGE
2.1	I vs. (1/T) shows a linear region between 8 and 9.5 K that may indicate an activation energy of about 12 meV.....	6
2.2	I versus 1/T data fits two activation energies .....	7
3.1	SRP qualifies the epi run showing the right concentration at the transparent contact as well as detecting layer .....	13
3.2	SRP at Solecon Laboratories performed at the end of the process confirms the desired epitaxial profile on the NASA 5 epi run.....	14
4.1	Wafer map of the CRC 778 IBC detector mask .....	21
4.2	Layout and bonding diagram of the CRC 603 fanout used to test the 128 x 128 detector arrays.....	22
5.1	Detector test station used to measure Signal and Noise .....	25
5.2	Dual Grating Diffraction Spectrometer measures relative spectral response from 0.2 to 30 $\mu\text{m}$ .....	26
5.3	Spectral response from three IBC arrays of different detecting region thickness show improved response at the lower wavelengths as the detecting thickness increases.....	29
6.1	Architecture of the CRC 744 readout .....	31
6.2	Signal path of the CRC 744 readout .....	32
7.1	Bonding diagram of the IBC SCAs (744/778).....	33
8.1	Gray plot of the quantum efficiency of SCA 011 .....	36

## TABLES

TABLE	TITLE	PAGE
2.1	Dark current density ( $J_d$ ) and other performance information on selected detectors from previously fabricated lots. ....	8
3.1	Number of wafers with the implemented arsenic concentration and epi thickness .....	9
3.2	Arsenic concentrations and implant energies used for the arsenic transparent contact experiment .....	11
4.1	The wafers selected for the three and six masking step lots .....	17
4.2	NASA wafers that were replaced.....	18
4.3	Wafers selected for further processing .....	19
5.1	Wafer screen tests performed to select the most promising epitaxial wafers for good dark current and Quantum Efficiency.....	24
5.2	Test results on the 18 parts fabricated in the program.....	27
7.1	SCA Assembly history .....	33
8.1	Six SCAs Tested.....	34
8.2	Biases and clock values used to test SCA 011. All other SCAs were tested in a very similar manner.....	35

## **ACRONYMS**

<b>DOE</b>	<b>Design of Experiment</b>
<b>IBC</b>	<b>Impurity Band Conduction</b>
<b>IRAC</b>	<b>Infrared Array Camera</b>
<b>MED</b>	<b>Microelectronics Division, Hughes, Newport Beach</b>
<b>NASA</b>	<b>National Aeronautics and Space Administration</b>
<b>SAO</b>	<b>Smithsonian Astrophysical Observatory</b>
<b>SBRC</b>	<b>Santa Barbara Research Center</b>
<b>SCA</b>	<b>Sensor Chip Assembly</b>
<b>SIRTF</b>	<b>Space Infrared Telescope Facility</b>
<b>SRP</b>	<b>Spreading Resistance Profile</b>

# **1 EXECUTIVE SUMMARY**

## **1.1 Program Objective**

In the past, the work on this technology addressed scanning applications, gain mode operation and operation at as high a temperature as possible (around 11.5 K). The Program objective of the 256 X 256 Si:As Impurity Band Conduction (IBC) detector development was to improve the sensitivity and performance of the large staring IBC detector arrays with an emphasis in understanding the dark current mechanism. We wanted to demonstrate operation of these arrays at very low cryogenic temperatures (<7K) and decrease the dark currents without degrading the quantum efficiency and uniformity of the devices.

A second objective was to verify the producibility of these IBC arrays in larger staring formats, 256 x 256 arrays with future growth to 1024 x 1024 arrays, than have been done previously. The 256 x 256 arrays are the formats needed for the Space Infrared Telescope Facility (SIRTF) program.

## **1.2 Program Approach**

The program followed the plan below:

- 1) Analyze existing Si:As IBC data and retest selected test structures to determine the most promising epi "recipes" that would result in low dark current detectors.
- 2) Based on the above analysis and tests, fabricate on at least 40 wafers a variety of Si:As IBC epitaxial layers at the Hughes facilities at Newport Beach, the Microelectronics Division (MED)
- 3) Select a variety of epi wafers and fabricate one lot of IBC detectors.
- 4) Dice at least 10 wafers, hybridize detectors from these wafers to fanouts and characterize the detectors for quantum efficiency, spectral response, noise and dark current.

5) Based on the tests above, hybridize detectors from the most promising wafers to CRC744 readouts purchased from the Smithsonian Astrophysical Observatory (SAO) program, test and deliver three Sensor Chip Assemblies (SCAs).

### 1.3 Program Execution.

Santa Barbara Research Center (SBRC) performed all the tasks in the original statement of work. SBRC analyzed and took data on detectors fabricated from six recent IBC lots and based on the data, prepared an epi growth plan of six epi runs parametrically changing the epi thickness, the arsenic concentration and the transparent contact impurity type, through a set of plausible values. In addition, the effort was supplemented by the SAO program for which three additional runs were planned.

We grew IBC epi layers on 96 high resistivity. We selected 35 wafers and processed two lots of IBC detectors one using a six and the second a three masking step process. From these we selected 14 (eight from the SAO program) wafers to complete the indium bump process.

All but two wafers were diced and 18 parts were hybridized to fanouts and tested. From these tests we found that only three NASA wafers and three SAO wafers had a residual impurity low enough to fully deplete the detecting layer and thus attain sufficiently high quantum efficiency. We fabricated six SCAs, two from each one of these NASA wafers using CRC744 readouts, tested them, and delivered the six SCAs to NASA Ames.

### 1.4 Experimental Results

The first epi runs fabricated had a residual impurity larger than  $3 \times 10^{12} \text{ cm}^{-3}$ , which made it impossible to fully deplete the detecting layer with biases lower than the breakdown voltage. Thus, only three NASA runs (and three SAO runs) provided detectors which could be fully depleted and achieve high quantum efficiency. The dark current measured on these parts is quite low and there is some evidence that the six masking step process results in detectors with larger activation energies at low temperatures and, therefore, considerably lower dark currents at 8K.

## 1.5 Future Activity

The next program should restudy and further analyze the data from some of the samples that were not fully depleted to extract additional information on the dark current mechanisms. We should repeat some of the epi variations we tried in this program with lower residual impurity concentration. In addition, the next program should look at the effects of a steeper As concentration transition between the detecting and the blocking region, a possible dark current and noise mechanism factors that we were not able to include in our study.

## 1.6 Cost and Schedule

This program was a fixed price contract and thus it was performed at cost. The funds did not allow us to perform all the tests we would have liked to do on all the samples we fabricated. Nevertheless, we fabricated more epitaxial wafers and fabricated two rather than one lot of detectors.

The delivery of the parts was about six months behind schedule, partly because of delay in growing the epi, the fabrication of two lots instead of one, technical problems that caused delays in testing the parts, and analysis of the complicated results.

## 2 INITIAL DATA ANALYSIS

The mechanisms which generate dark current in IBC detectors at low temperatures are not well understood. This is due to (1) the complexity of the physics needed to model the possible dark current mechanisms and (2) the difficulty in performing experimental measurements which would provide the values of the physical parameters to insert in such models. Consequently we approached the problem in an heuristic fashion. From first order physical principles we expect the dark current to depend on at least several parameters. Arsenic concentration determines the average distance between arsenic atoms to each other and to compensating impurity atoms, hence affecting the average ionization energy, hopping mobility and average coulomb attraction between impurity band hole and compensating site. These effects may play a role in generating dark current. Increased electric field strength also lowers the ionization energy and may cause additional effects which generate dark current. It is also possible that detector processing can affect dark current through poorly understood mechanisms.

Consequently we spent the first three months of the program selecting which recent IBC lots that had already been tested would be relevant towards the understanding of the dark current effects. We selected six lots, some because they showed low dark current, including one lot (CRC 591) that had been successfully tested at NASA Ames; others because they had been extensively characterized.

In parallel, we prepared the hardware to test the dark current on those detectors for which that data had not been taken, and measured lower dark currents than we have taken in the past. The tests were performed on a capped multi-chip dewar. At this initial stage we performed two tests, a I-V test at 10 and 8K to understand the breakdown properties and an I vs.  $(1/T)$  from 8 to 14K to study the activation energies.

We measured activation energies of about 22.2 meV above 10K and 14 meV below 10K on a couple of samples. These measurements were limited by the electrometer, which could reliably only measure down to  $5 \times 10^{-15}$  A. The fanouts we used to measure the dark current combine in parallel arrays of either  $10 \times 10$  or  $21 \times 21$  30 square micron pixels. Thus, the lowest current density we are able to measure reliably is

between 2 and 5 E-12 A/cm<sup>2</sup>. This value of the current density is higher than the expected dark current at 8K. Thus, some of the dark currents listed at that temperature were probably limited by the measuring system.

Figure 2.1 shows the I vs. (1/T) measurement which was used to calculate the activation energies. This specific test die from wafer seven of lot 639 - 3, fabricated on IR&D in 1991, resulted in the lowest dark current measured. The breakdown voltage on this part is about 3 volts at 8K. Figure 2.2 shows data from a test die from the 784 lot. This lot had higher dark current than the other test die, but the data fit very well at two activation energies - 22.2 meV above 10K, and 14 meV below 10K.

Table 2.1 shows the results of the entire data measurement and analysis. The column titled "new dark current test," lists all the additional data taken in this initial program task. We considered the effects of different detecting epitaxial thicknesses, transparent contact types and concentrations, As concentrations and residual doping impurity concentrations on the dark current. However, the results, when sorted for different epi runs and resulting dark currents, did not give any clear indication of what needed to be done to get lower dark current, except to lower the residual impurity concentration of the detecting layers.

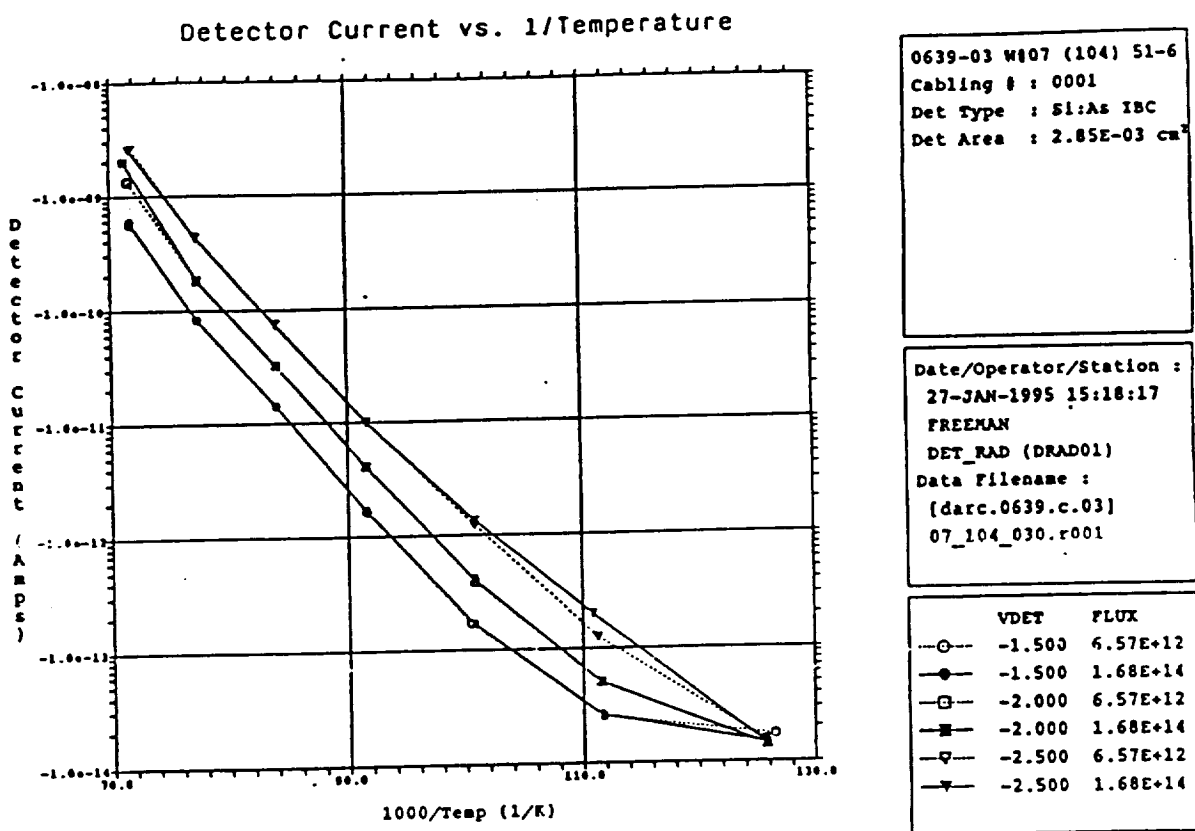


Figure 2.1 The log plot of the I vs. (1/T) shows a linear region between 8 and 9.5 K with an activation energy of about 12 meV.

Si:As IBC, 0784-01-31-001, Diode 15

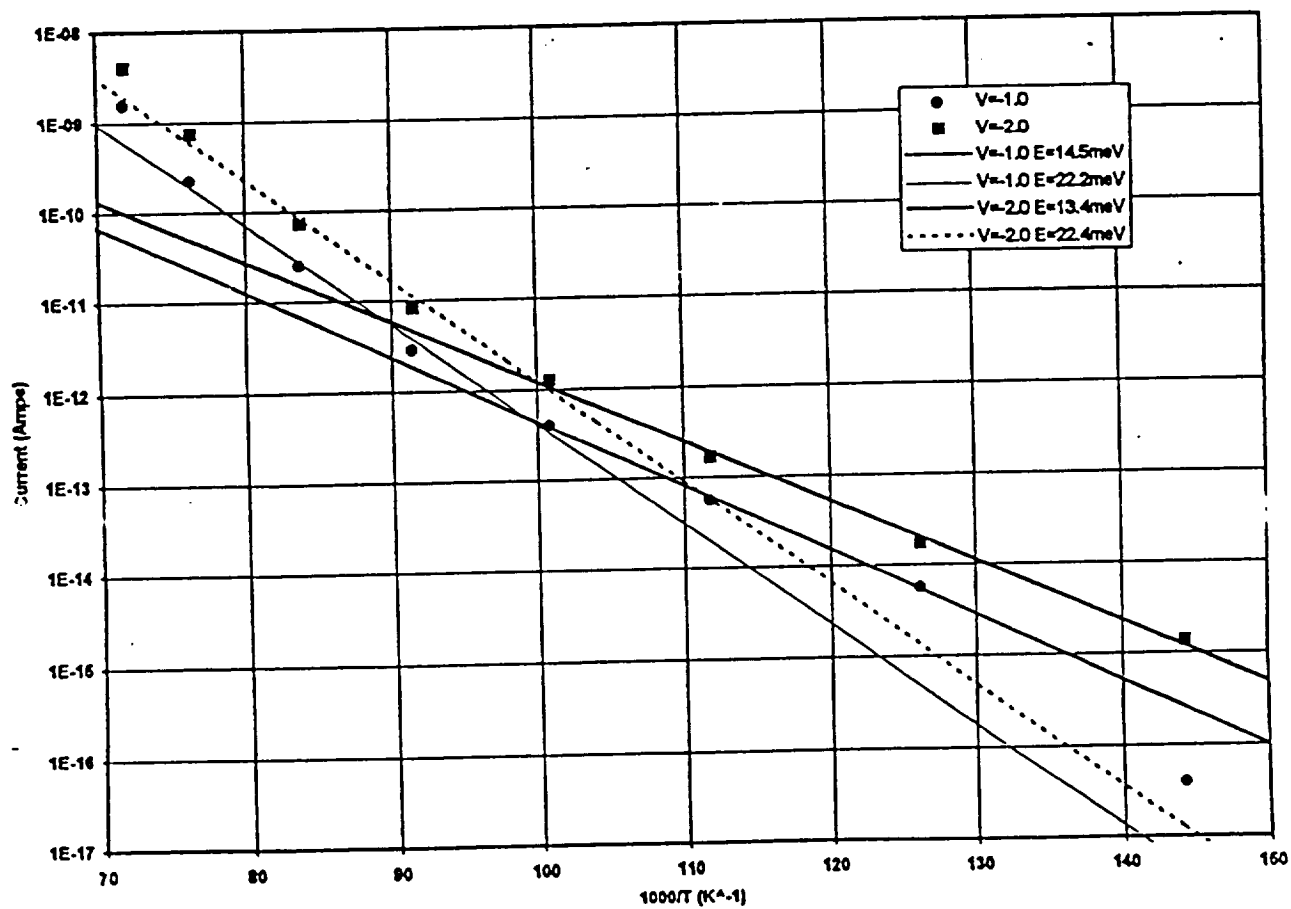


Figure 2.2 The log plot of  $I$  versus  $1/T$  data fits two activation energies.

**Table 2.1 Dark current density ( $J_d$ ) and other performance values on selected detectors from previously fabricated lots**

Wksht.xls

Part Identification				Dark Current Data										Jd @ 5K				Material Data						
				Dark current density at 10K (pA/sq.cm)																				
				New Dark current tests																				
Lot	Water	Die	Test seq	Full depletion bias	Bias	Magnitud	10K-8K act. energy (meV)	Bias	Magnitud	10K-8K act. energy (meV)	Bias	Magnitud	10K-8K act. energy (meV)	E1 @ 1V	E2 @ 1V	Jd @ 5K	J @ 8K	source (NB, 1200, 800)	Profile G-graded S-Step F-flat	As conc. (e17)	thick (um)	N comp (e12)	Back Impl (Yes No)	
784-1	19	2	1	-2.5	-1	23		-2	77		-2.5	129												Y
784-1	31	1	2	-2	-1			-1.5	11		-2	76		12.9	29.1	4.0E-17								Y
707-1	1	204	6	-0.8	-1.5	23		-2.5	101										s	3.5	29	0.8		
707-1	1	204	6	-0.8	-1.5	23		-2.5	101										s	3.5	29	0.8		
707-1	13	205	1	-0.9	-1.5	59		-2.5	246					12.6	29.3	5.7E-16	3.4E-11		s	4.5	30	0.8	See anti	
707-1	14	205	1	-0.9	-1.5	285		-2.5	1110					5.5	31.5	3.7E-13	4.0E-11		same as above					
707-1	18	204	3	>-3	-3	1630		-4	6390	17									s	4.6	38	3		
707-1	24	204	4	-0.6	Appears to have large dark current!														s	4.7	31	0.7		
707-1	24	205	3				Same as above							17	33.4	2.5E-18	6.8E-12							
707-1	24	205	3				Same as above							16.3	32.6	5.5E-18	8.7E-12							
707-1	30	204	3	-4	-2	86*		-3	308*		-4								s	3.5	38	2.5		
707-1	34	204	3	-1	-1.5	17		-2.5	63										s	3.6	30	1		
707-1	39	204	1		-1.5	46000	12	-2.5	595000	11	-3	2E+06	11						s	3.6	36	107		
707-1	43	205	2		-1.5	160		-2.5	596		-3	1365							same as above					
707-1	48	205	1	-1	-1.5	952		-2.5	3387										s	3.6	30	2		
707-1	52	204	4	-2	-1.5	164*		-2.5	504*										s	3.7	38	2		
778-1	5	2	6	-1	-1.5	180		-2	331		-2.5	675	17					NB	s	5.7	27			
778-1	5	2	6	-2	-1.5	256		-2	507		-2.5	1028		16.1	29.9	3.8E-18	4.4E-12	NB	s	5.7	29	2.5		
778-1	5	2	6	-2	-1.5	256		-2	507		-2.5	1028		11.8	22.9	2.7E-16	8.2E-12	NB	s	5.7	29	2.5		
778-1	7	1	6	-1.7	-1.5	273		-2.5	789		-3	1334	17					NB	s	4.6	37	1.2		
778-1	9	1	8	-1.6	-1	244		-2	721		-2.5	1196	16	14.4	29.7	8.9E-17	2.3E-11	NB	s	5.6	37	1		
778-1	9	1	8	-1.6	-1	244		-2	721		-2.5	1196	16	12.3	20.2	4.9E-16	2.4E-11	NB	s	5.6	37	1		
707-2	14	204	2	>>-2	-0.75	12700		-1	24500	11	-2	1E+06	12					800	l	7	28	45	y	
707-2	14	205												11.4	24.6	3.1E-13	6.3E-09	800	l	7	28	45	y	
707-2	14	205												10.7	26.2	5.7E-13	6.3E-09	800	l	7	28	45	y	
707-2	16	204	3	>-3	-0.75	2200		-1	6000		-2	75000		7.89				800	s	3.6	27	100.4	y	
707-2	23	204	3		-0.75	1940	7	-1	3130	6	-2	401000	12	7.98				800	s	4.8	26	30	y	
707-2	23	204																						
707-2	28	301	4	NA	-0.5	22		-0.75	39		-1	90		10.7				2.4E-10	NB	s	4.7	39	0.8	n
707-2	28	301	4	NA	-0.5	22		-0.75	39		-1	90		10.7				1.1E-09	NB	s	4.7			n
707-2	30	301	4	-2	-0.5	79	NA	-1	198	NA	-1.5	351	NA	11.7	26.2	1.7E-14	4.3E-10	NB	s	4.7	38	1	y	
707-2	30	301	4	-2	-0.5	79	NA	-1	198	NA	-1.5	351	NA	11.7	26.2	1.9E-14	4.6E-10	NB	s	4.7			y	
707-2	33	301	5	-1.6	-0.75	63	NA	-1	86	NA	-2	45700	18					NB	s	4.6	30	1	n	
707-2	34	309	6	-1.5	-0.75	164	NA	-1	231	NA	-2	633	NA					NB	s	4.6	30	1	y	
639-1	2	4	24	-1.2	-1.5	<19	NA	-2	-21	NA	-2.5	<27	NA					800	l?	5	27	1.5	n	
639-1	7	3	62	-1	-1	6	NA	-1.5	8	NA	-2.5	22	NA					800	g	3.7	28	1.5	y	
639-1	9	6	22	-1				-2	31	NA								800	g	3.6	24	1.2	y	
639-3	7	104	7	-2.5	-1	28	NA	-2	120	NA	-2.5	269	NA	17.8	30.8	6.4E-20	5.3E-12						4	
639-3	7	104	7	-2.5	-1	28	NA	-2	120	NA	-2.5	269	NA	10.8	25.7	1.1E-16	6.0E-12						4	
639-3	9	103	3	-3	-1	38	NA	-2	188	NA	-2.5	453	NA	10.8	25.7	1.1E-16	3.7E-12						3	
639-3	9	103	3	-3	-1	38	NA	-2	188	NA	-2.5	453	NA	10.8	25.7	1.1E-16	1.5E-12						3	

### 3 EPITAXIAL GROWTH

#### 3.1 Epitaxial Wafer Selection

We selected a number of epitaxial runs to optimize and learn the behavior of the dark current as a function of the epitaxial growth parameters. We chose the 25  $\mu\text{m}$  epi with an arsenic concentration of  $5 \times 10^{17} \text{ cm}^{-3}$  as the baseline. The strategy was to investigate the effect of arsenic concentration and epi thickness on the dark current. We prepared a set of parametric experiments around the baseline and changed, one at a time, the key parameters that we thought would affect the dark current. Table 3.1 lists the selected epitaxial layers.

**TABLE 3.1 Number of wafers with the arsenic concentration and epitaxial thicknesses selected for this investigation.**

<b>RUN NUMBER</b>	<b>ARSENIC CONCENT. (<math>\times 10^{17} \text{ cm}^{-3}</math>)</b>	<b>THICKNESS (MICRONS)</b>	<b>NUMBER OF WAFERS</b>
<b>Sb Transparent Contact</b>			
<b>BASELINE</b>	<b>5</b>	<b>25</b>	<b>16</b>
<b>NASA2</b>	<b>5</b>	<b>15</b>	<b>8</b>
<b>NASA3</b>	<b>3</b>	<b>25</b>	<b>8</b>
<b>NASA4</b>	<b>7</b>	<b>15</b>	<b>8</b>
<b>As Transparent Contact</b>			
<b>NASA5</b>	<b>5</b>	<b>25</b>	<b>8</b>
<b>NASA6</b>	<b>5</b>	<b>25</b>	<b>16</b>

Starting with the baseline thickness, we decreased the thickness to 15  $\mu\text{m}$  (runs NASA 2 & 4). The parallel SAO program needed 35  $\mu\text{m}$  epi to optimize operation at 6.3 and 8 microns. Thus, we did not increase the thickness to investigate the effect of thicker layers - the SAO runs would provide this information. To conserve the high quantum efficiency we increased the arsenic concentration in run NASA 4. We also decreased the arsenic concentration from

5 to  $3 \times 10^{17} \text{ cm}^{-3}$  to see if lower concentration improved the dark current, even if it was at the expense of lower quantum efficiency.

We also wanted to investigate the dark current properties of arsenic transparent contacts. Arsenic has a higher activation energy than Sb, thus it is possible that the As contacts may result in lower dark current. Nevertheless, As diffuses much faster in Silicon than Sb. During the hot etch in the epitaxial reactor, necessary to prepare the wafers for a clean and defect-free epi growth, the diffusion broadens the As concentration. This requires a heavier dose of As to keep the peak concentration above the metal-insulator transition and avoid freeze out of the contact. The result is a higher absorption in the contact and lower quantum efficiency.

We tried two runs using the As contacts; the first, NASA 5, with the regular "in situ" etch, and a second, NASA 6, with only the etch due to the natural oxide grown on the surface of the wafer, about  $200 \text{ \AA}$ . The etched run could result in lower quantum efficiency, because of possibly poor electrical contacts as the etch removes the implanted arsenic, but better crystal quality, while the non etched wafers (or minimally etched wafers) should result in higher quantum efficiency but possibly poorer epi layers with more crystallographic defects.

Table 3.2 shows the number of wafers that we implanted with As and the implant concentrations and energies used.

**TABLE 3.2 Arsenic concentrations and implant energies used for the arsenic transparent contact experiment.**

<b>RUN NUMBER</b>	<b>ARSENIC DOSE (<math>\times 10^{14} \text{ cm}^{-2}</math>)</b>	<b>IMPLANT ENERGY (keV)</b>	<b>NO. OF WAFERS ETCHED</b>	<b>NO. OF WAFERS NON- ETCHED</b>
<b>a</b>	<b>5</b>	<b>55</b>		<b>2</b>
<b>b</b>	<b>7</b>	<b>55</b>		<b>2</b>
<b>c</b>	<b>7</b>	<b>80</b>	<b>4</b>	<b>2</b>
<b>d</b>	<b>7</b>	<b>120</b>		<b>4</b>
<b>e</b>	<b>12</b>	<b>80</b>	<b>4</b>	<b>2</b>
<b>f</b>	<b>12</b>	<b>120</b>		<b>4</b>

### 3.2 Epi Growth

The first step in the epi growth process is to grow as many 8  $\mu\text{m}$  epi layers on high purity silicon wafers as needed, until we prove that the residual impurity concentration is below  $2 \times 10^{12} \text{ cm}^{-3}$ . We achieved a purity of about  $1 \times 10^{12} \text{ cm}^{-3}$  before we started growing the epitaxial layers.

The next step are the calibration runs. Prior to growing the program epi we need to calibrate: (1) the etch rate, to know exactly how many Angstroms of silicon we need to remove from the surface of the wafers, (2) the epi growth rate and the uniformity calibration, and (3) the flows and temperatures setting to achieve a desired arsenic concentration.

From the Spreading Resistance Profile (SRP) measurements on calibration runs we noticed that some wafers had lower Sb concentration in the contact than we desired, so we sent half the wafers for an additional Sb implant at Krokos (a small company in Tustin, California, which SBRC and Hughes has used extensively for special implants) to assure that we had a sufficiently high concentration at the surface of the wafer prior to epi growth. A poor transparent contact, either too high or too low a Sb concentration, could make the detectors inoperable.

The epi wafers were all fabricated in April 1996 and delivered to SBRC for processing on 1 May. SRP measurements indicated that all the lots were processed correctly, the desired thicknesses were achieved between +/- 1  $\mu\text{m}$ , the As concentration in the detecting layer was achieved within ten percent of the desired value, the blocking layer reached the  $1\text{E}14\text{ cm}^{-3}$  desired concentration, and the buried transparent contacts had the desired Sb concentration. Figure 3.1 shows the profile measured on a test wafer after growing the detecting layer. These measurements were performed at MED. Figure 3.2 shows the measurements on the completed run, including the blocking layer. These SRP measurements were performed at Solecon Laboratories (Tustin, California) a company that specializes in testing materials and wafers. These tests confirmed the work and measurements performed at MED.

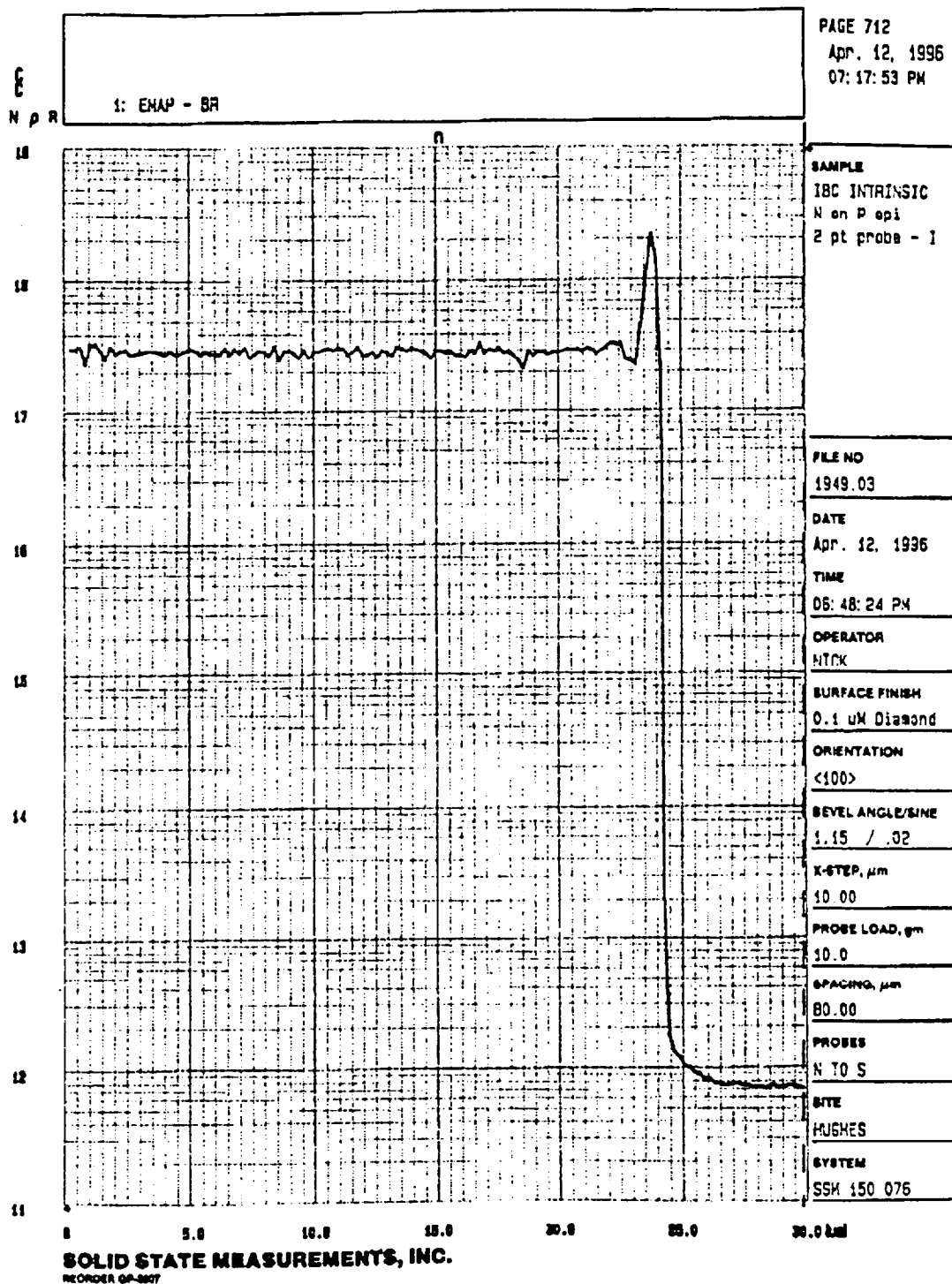


Figure 3.1 SRP qualifies the epi run by showing the right concentration at the transparent contact and at the detecting layer.

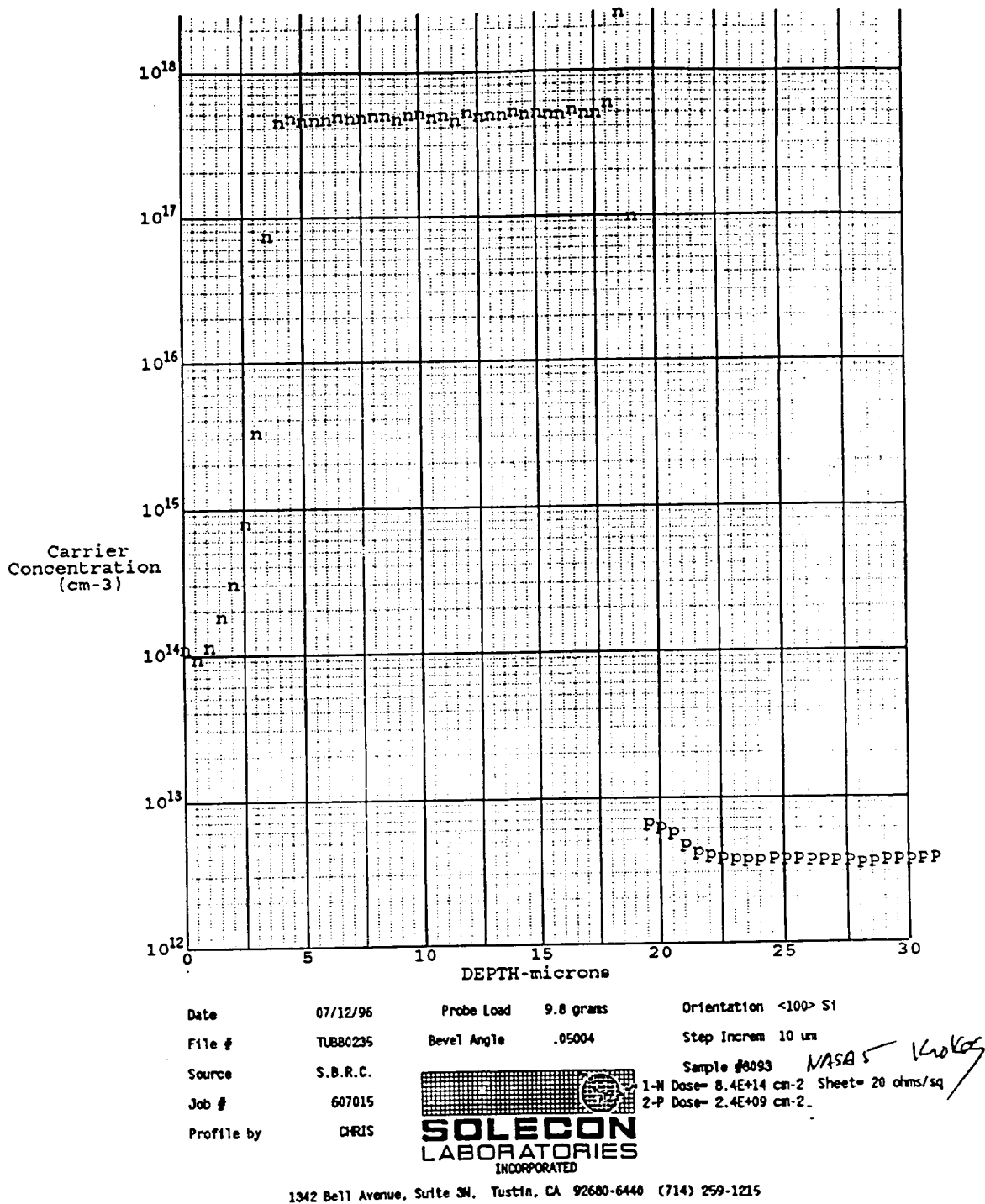


Figure 3.2 SRP at Solecon Laboratories, performed at the end of the detector process, confirms the epitaxial profile on the NASA 5 epi run.

In addition to the work detailed above, we fabricated three epi runs for the IRAC program. The IRAC runs emphasized thicker epi layers with higher As concentration to optimize operation at the lower wavelength bands (6 to 8 microns). These epi runs were fabricated under the SAO contract.

## **4 DETECTOR FABRICATION**

### **4.1 Wafer Selection**

There was some evidence that the simplified three masking process step, an exact subset of the standard SBRC six masking step, resulted in better dark current. An IBC detector tested at NASA Ames that had very low dark current came from a three masking step lot. Thus, we wanted to test this theory. Table 4.1 lists the wafers we selected for the three and the six masking step lots.

The primary difference between the 3 and 6 masking step processes is in the way pixels are delineated. The three masking step process uses the simpler approach of etching into the silicon between the pixels. The 6 masking step implants a heavily doped channel stop between the pixels which then is passivated with an oxide layer. In principle the 6 masking step process should yield a better passivated surface.

The first column of Table 4.1 identifies the epi run type. In addition to choosing the wafers fabricated in this program, we added wafers from the SAO program and other inventory wafers, used in previous IBC lots (the CRC778 and the CRC707 lots), that resulted in very low dark current detectors.

The second and third columns list the specific wafers selected for the three and the six masking step process.

As stated above, half the wafers were sent to Krokos for an extra implant to assure that the transparent contact peak concentration was sufficiently high that it did not freeze at 5K. The fourth column identifies those wafers that have received this additional implant.

The epitaxial information we have available for each of the runs is listed in the next three columns and applies to all the wafers of that particular run.

The final column lists the design parameters. Comparing these numbers to those in the previous three columns we can see that MED met, as much as we could tell at that time, all the specifications.

The runs identified as NASA 1 and 2 have wafers with a variety of Arsenic transparent contacts, as shown in Table 3.2

**TABLE 4.1 The wafers selected for the three and six masking step lots include wafer from all the epi varieties.**

All of these wafers have been cleaned and a photoresist coat has been applied to the epi side to protect the surface while we polish the opposite side of the wafer.

TABLE II - LOT WAFERS FOR THE 3 AND 6 MASKING STEPS							
EPI run	Wafer Numbers	Wafer Numbers	Implanted at Krokos?	Actual Concentration	Actual thickness	Actual Contact	Design parameters (concn/thickn)
	3 MS	6 MS					
NASA 1	8142		YES	5.0E+17	25		5E17/25
	8144		YES				As contact
	8146		YES				
	8153		YES				
NASA 2	8148		YES	5.0E+17	25		5E17/25
	8157		YES				As Contact
	8158		YES				
	8163		YES				
NASA 3	8094	8095	NO				3E17/25
NASA 4	8082	8083	YES	5.0E+17	24		5E17/25
	8075	8076	NO				BASELINE
NASA 5	8092	8091	YES	5.0E+17	15		5E17/15
	8086	8087	NO				
NASA 6	8120	8122	YES				7E17/15
	8118	8117	NO				
SAO 1	8108	8106	YES	5.0E+17	35	3.2E+18	5E17/35
	8102	8103	NO				
	8109	8110	YES				
SAO 2	8130	8131	NO				7E17/25
	8126		YES				
SAO 3	8139	8137	YES				7E17/35
	8135	8132	NO				
	8140	8141	YES				
WAFERS FROM EXISTING INVENTORY							
778-1	8008			5 TO 7 E17	29		
	8018						
	8026						
	8037						
707-2	RUN 1-AVO-1-12			4 TO 7 E17	27-30		
	RUN 2-AVO-1-01						
	RUN 3-AVO-2-04						
	RUN 4-AVO-2-08						

## 4.2 Detector Wafer Processing

The 45 wafers selected for processing, listed in Table 4.1, were back-polished and underwent the three and six processing steps. Seven wafers from the initial three masking step lot (and six SAO wafers) were improperly etched, destroying the entire epi region. This was due to using a smaller beaker to etch the wafers. We replaced these wafers with other wafers from the same epi runs. The initial process steps of the 13 wafers was accelerated to catch up with the rest of the lot. Table 4.2 lists the wafers that were lost at the etch step and the replacement wafers.

**Table 4.2 NASA wafers that were replaced**

<b>EPI RUN</b>	<b>WAFER LOST</b>	<b>WAFER REPLACED</b>
<b>NASA 1</b>	<b>8146</b>	<b>8147</b>
<b>NASA 2</b>	<b>8148</b>	<b>8149</b>
	<b>8157</b>	<b>8158</b>
	<b>8165</b>	<b>8164</b>
<b>NASA 4</b>	<b>8082</b>	<b>8084</b>
<b>NASA 6</b>	<b>8120</b>	<b>8121</b>
	<b>8118</b>	<b>8119</b>
<b>707-2</b>		<b>WAFER 7</b>
<b>(SAO1</b>	<b>8108</b>	<b>8111</b>
<b>SAO2</b>	<b>8130</b>	<b>8129</b>
<b>SAO3</b>	<b>8139</b>	<b>8138</b>
	<b>8140</b>	<b>8136</b>
<b>778</b>	<b>8037</b>	<b>8038)</b>

## 4.3 Back End Processing

The two lots, three and six masking steps, were completed in August 1996. From the 45 wafers that completed processing we selected 20 wafers to continue with indium bumps, dicing and hybridizing detector die to fanouts for full detector characterization. Table 4.3 lists the wafers selected for further processing. The selection criteria was to chose the wafers that better represented the experimental parametric matrix that we generated at the beginning of the program (see section 3.1). If

necessary, based on data taken on the selected wafers, we would go back and process other wafers.

**Table 4.3 Wafers selected for further processing**

<b>WAFERS TO BE POLISHED &amp; SENT FOR INDIUM BUMPS</b>					
<b>WAFER</b>	<b>LOT</b>	<b>EPI run</b>	<b>Epi</b>	<b>As epi layer</b>	<b>Comments</b>
<b>NUMBERS</b>	<b>NUMBER</b>		<b>Thickness</b>	<b>Concentration</b>	
			<b>(<math>\mu\text{m}</math>)</b>	<b>(<math>\times\text{E}+17</math>)</b>	
<b>LOT 11 D (FIRST 10 WAFERS TO BE PROCESSED)</b>					
8011	11	778-1	29.0	5 to 7	
8084	11A	NASA4	24.0	5.0	BASELINE
8092	11	NASA 5	15.0	5.0	
8111	11A	SAO 1	35.0	5.0	BASELINE
8121	11A	NASA 6	15.0	7.0	
8129	11A	SAO2	25.0	7.0	
8135	11A	SAO3	35.0	7.0	
8142	11	NASA 1	25.0	5.0	As contact
8164	11A	NASA 2	25.0	5.0	As Contacts (Etched)
AVO # 7	11	707-2	30.0	4 TO 7	
<b>LOT 11 E (SECOND 10 WAFERS TO BE PROCESSED)</b>					
8026	11	778-1	29.0	5 TO 7	
8075	11	NASA 4	24.0	5.0	BASELINE
8083	12	NASA 4	24.0	5.0	BASELINE
8094	11	NASA 3	25.0	3.0	
8102	11	SAO 1	35.0	5.0	BASELINE
8106	12	SAO 1	35.0	5.0	BASELINE
8122	12	NASA 6	15.0	7.0	
8131	12	SAO2	25.0	7.0	
8137	12	SAO 3	35.0	7.0	
8156	11A	NASA 2	25.0	5.0	As Contacts (Etched)
<b>NOTES</b>					
1	Lot 11 are wafers from the three masking step lot				
2	Lot 11A are the wafers that were replaced on the three masking step lot				
3	Lot 12 are wafers from the 6 masking step lot				
4	Wafers XXX and YYY are being held for photoresist rework				

We had difficulty applying photoresist onto two of the wafers. The apparent reason is that the large groove etches needed to contact the transparent back contact caused a bubble and the photoresist could not be removed. The remaining 18 wafers were properly processed and partially diced.

The mask set used to process this lot was a SBRC owned mask set (CRC 778) which contained a variety of array configurations. Figure 4.1 shows the detector wafer map. The desired arrays for the program are the 256 x 256 arrays that occupy less than a quarter of the wafer. Therefore, because we had available fanouts for the 128 x 128 array configuration (CRC 603 lot), we choose the die marked A, B, and C in Figure 4.1 to be hybridized to fanouts and used for detailed detector tests. All 18 wafers were partially diced to retrieve the three arrays (A, B, and C). From past experience we expect all the die from the same wafer will exhibit essentially the same behavior

The fanout layout is shown in Figure 4.2. We hybridized one array from each of the 18 wafers to the fanouts.



FANOUT #: 603C

AREA/PIXEL= 5.625E-5CM2

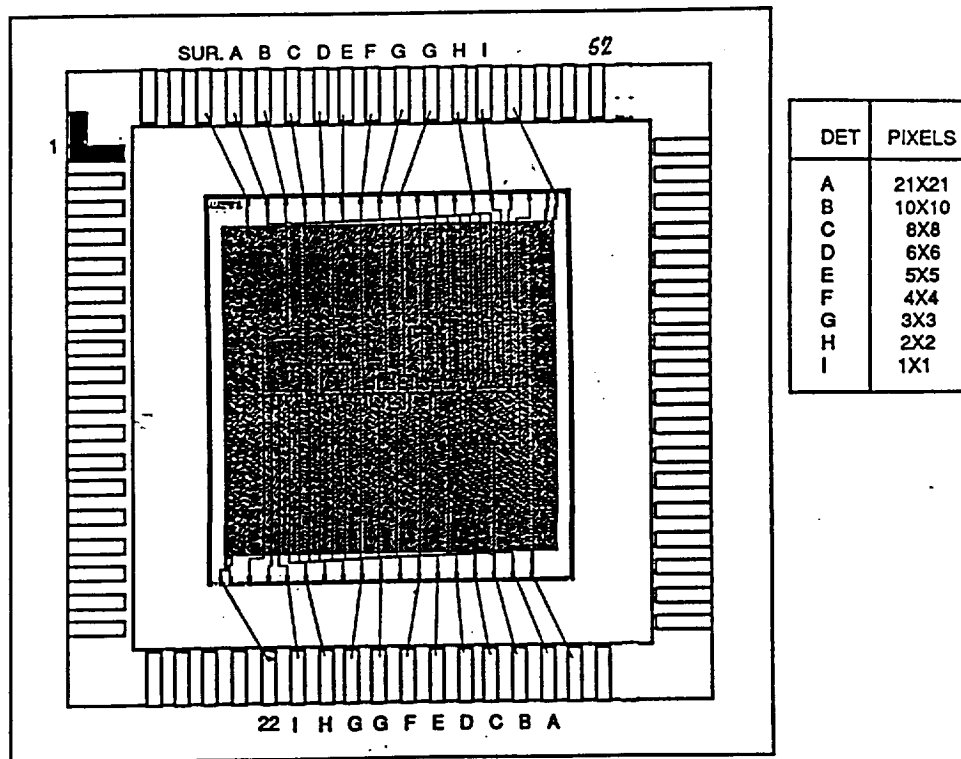


Figure 4.2 Layout and bonding diagram of the CRC 603 fanout used to test the 128 x 128 detector arrays

## **5 Detector Test**

### **5.1 Test Preparation**

Most of the tests that we wanted to perform were already done at the beginning of the program (Section 2) and, therefore, most of the test preparation had also been done. An unexpected complication was the use of 68 pin packages with a wider well needed to accommodate the larger 128 x128 test arrays. We fabricated an adapter for the optical stack. In addition, we broke a couple of packages when we applied the pressure needed to assure that the part is in contact with the cold finger.

We proceeded to measuring the dark current first, but we soon realized that the data could not be analyzed until we had a complete set of detector measurements including the depletion and breakdown voltages and the signal, to know that the detectors behaved correctly. The dark current tests were repeated on those parts that showed good behavior.

### **5.2 Detector Test Facilities**

The selection of the optimum detector wafers is based primarily on quantum efficiency and dark current. A key parameter for the optimum operation of the IBC detectors is the knowledge of the full depletion voltage, which tells us the concentration of the residual purity and the breakdown voltage. This is measured by performing capacitance versus voltage. At full depletion the capacitance of the detectors does not increase with voltage. The spectral response is taken on a few parts.

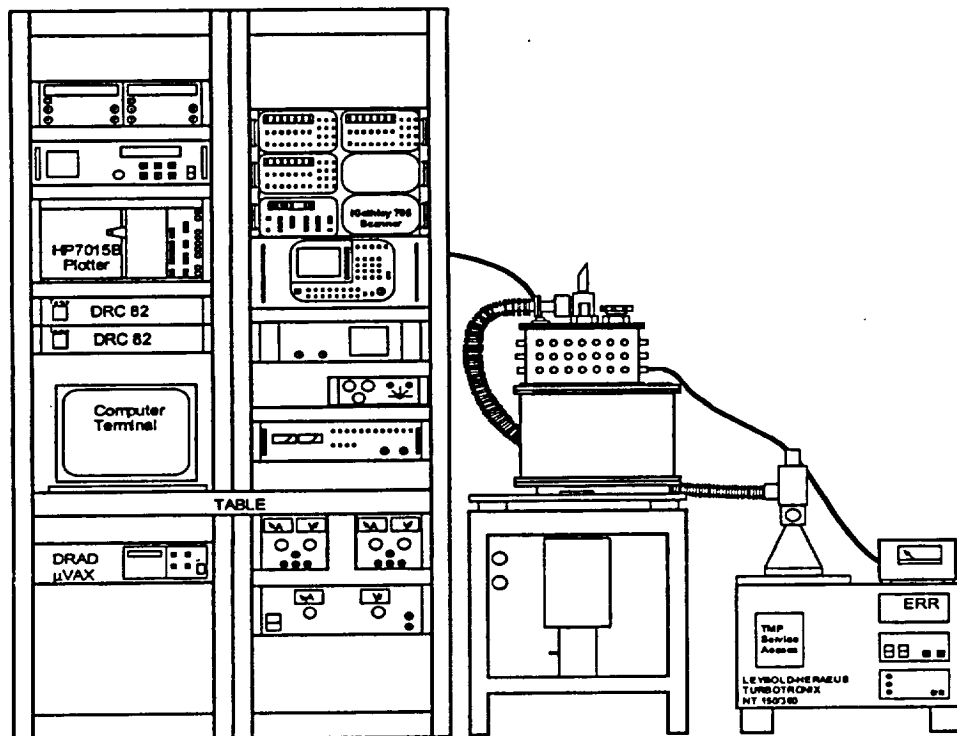
The actual tests performed on the detector test die are shown in Table 5.1. All tests are performed on all the samples except the spectral response which is performed only on selected parts.

**Table 5.1 Wafer screen tests performed to select the most promising epitaxial wafers for good dark current and quantum efficiency.**

<b>TEST</b>	<b>RESULT</b>
<b>I vs <math>A_j^*</math> 10K, 0 FOV</b>	<b>Identify Valid Pixel Group</b>
<b>I vs V 10K, 0 FOV</b>	<b>Dark Current, Breakdown Voltage</b>
<b>C vs V 10K, 0 FOV</b>	<b><math>N_c</math> and Full Depletion Voltage</b>
<b>I vs V 10K with Flux</b>	<b>Response vs Voltage, Peak QE</b>
<b>Spectral 10K (at Full Depletion)</b>	<b>QE vs Wavelength</b>
<b>I at 8K, 0 FOV (at Full Depletion)</b>	<b>Dark Current</b>
<b>I vs T</b>	<b>Temperature Dependence and Activation Energy</b>

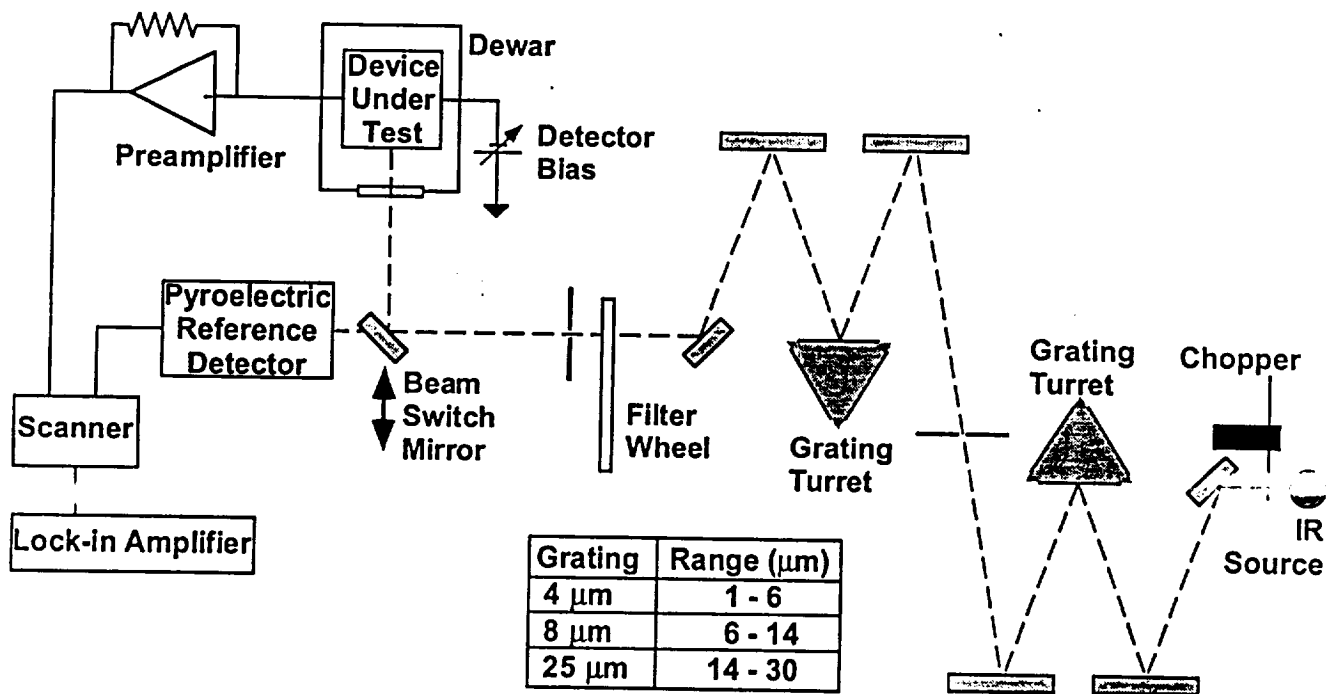
\* $A_j$  = Area of detectors

Figure 5.1 shows the typical detector test station we used to characterize the detector test structures. The station consists of power supplies, Keithley electrometer, and function generators. The station is computer control from a MicroVAX computer. We have two dewars - a standard one chip dewar and a multichip dewar that allows us to test 12 detector test chips at a time.



**Figure 5.1 Detector test station used to measure Signal and noise.**

The spectral response is measured on a dual grating diffraction spectrometer by using three different gratings to measure the relative spectral response from 2 to 30  $\mu\text{m}$ . The spectra have been measured with this system. Figure 5.2 shows the schematic of the spectral station. Eighty-five percent of the documentation needed to be fully compliant with the ISO 9001 guidelines was completed while testing these arrays.



**Figure 5.2** Dual Grating Diffraction Spectrometer measures relative spectral response from 2 to 30  $\mu\text{m}$ .

Table 5.2 Shows the results obtained on the 18 parts that we tested.

**Table 5.2 Test results on the 18 parts fabricated in the program**

Process				Test Results					SCA
Epi Run	Thick	As Conc	Mask	N <sub>c</sub>	V <sub>full dep</sub>	8K Dark <sup>2</sup>	10K Dark <sup>2</sup>	QE <sub>peak</sub> x G <sup>3</sup>	
	μm	10 <sup>17</sup> /cm <sup>3</sup>	Steps	x10 <sup>12</sup> /cm <sup>3</sup>	Volts	elec / sec	elec / sec		
778-1	26	5-7	3	2.1	1.3	144	9811	0.47	Yes
NASA 4	24	5	3	8.1	4.51		X		
NASA 4	24	5	6	6.7	3.71	X	X		
NASA 4	24	5	3	6.2	3.41		X		
NASA 3	25	3	3	8.7	5.21	X	X		
SAO 1	35	5	3	7.6	7.11		X		
SAO 1	35	5	6	8.9	8.31		X		
SAO 1	35	5	3	6.3	6.91		X		
NASA 6	15	7	3	2.6	0.6	134	2545	0.47	Yes
NASA 6	15	7	6	3.8	0.9	22	5210	0.43	Yes
SAO 2	25	7	3	2.1	1.2	287	2775	0.44	Yes
SAO 2	25	7	6	2 - 8	2	49	13693	0.56	Yes
SAO 3	35	7	3	1.7	2	144	49724	0.52	Yes
SAO 3	35	7	6	1.6	2	51	15223	0.5	Yes
NASA 2	25	5	3			Shorted			
NASA 2	25	5	3	7.7	4.61		X		
707-2	30	4-7	3	9	7.51		X		
Standard	25	4-7		0.72	0.8		12191	0.45	

- 1 - Projected Full Depletion Voltage Based on N<sub>c</sub> and Epi Thickness
- 2 - Dark Current (elec / sec) at Full Depletion Scaled to 30 μm Pixel
- 3 - Peak Quantum Efficiency x Gain (~1) at Full Depletion
- X - Data Exists, Valid Measurement at Full Depletion Voltage Not Possible

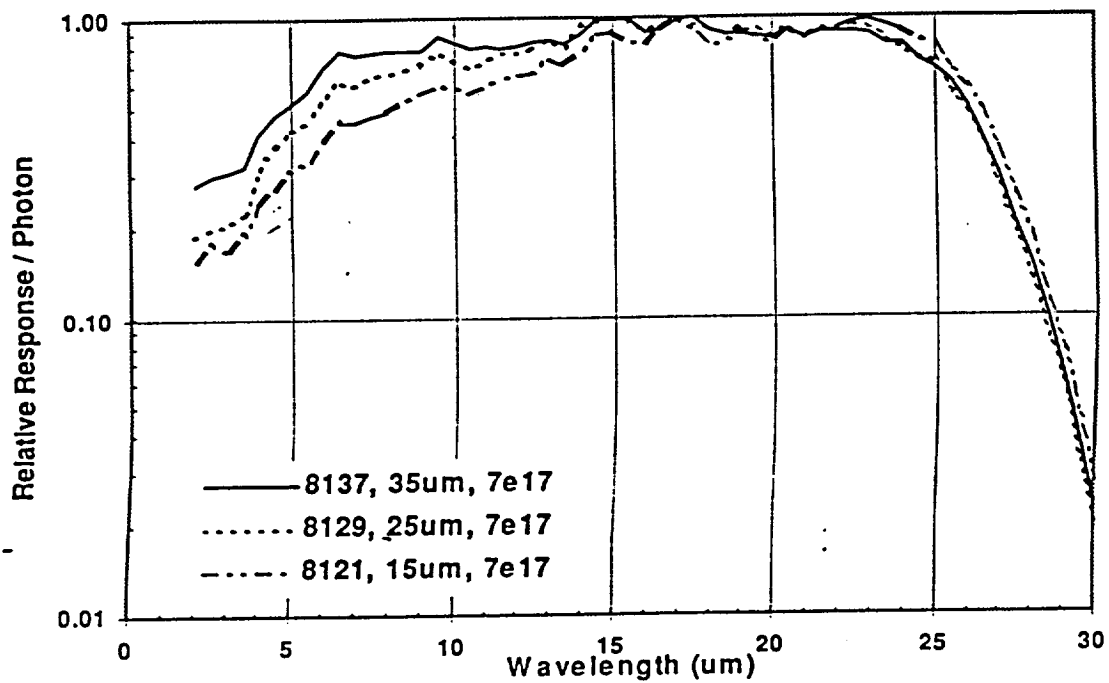
### 5.3 Detector Test Results

The first data that we analyzed from the capacitance measurements was the residual impurity, which ranged from a high of 9E12 cm<sup>-3</sup> to as low as 1.6 E12 cm<sup>-3</sup>. The parts with the high residual impurity could not be fully depleted before we reached the breakdown voltage and, therefore, we could not use them for valid and meaningful dark current measurements. The values of these parts are shown as dark in Table 5.2.

We found a correlation between the chronological order in which the epi layers were grown and the residual impurity level. We have not previously seen this effect. As a matter of fact we expected the opposite effect, that as we grew more epi runs after the initial clean, the epi would become contaminated. Typically we cleaned the reactor after 8 to 12 epi runs. This indicates that either the arsine line was contaminated and it cleaned itself as we grew more layers or perhaps a contamination occurred from a dirty wafer or other source prior to starting the program epi runs. The runs done at the end resulted in better parts than those done at the beginning. This inverse relation between purity and order of fabrication is not expected and we do not think this observation is scientifically relevant.

We also measured the signal response of the detectors through a spike filter centered at  $7.25\text{ }\mu\text{m}$  that was fully depleted and calculated good responsive quantum efficiencies, greater than 40 percent.

Three detectors were selected for spectral response. Figure 5.3 shows the spectral response of three arrays of different thickness. The response is what one would expect, as the thickness increases the response at the lower wavelengths improves.



**Figure 5.3 Spectral response from three IBC arrays of different detecting region thickness show improved response at the lower wavelengths as the detecting thickness increases.**

## 6 Readouts

For this program, we purchased two CRC 744 readout wafers from the SAO program. These were wafers 7 and 21. Wafer 7 was fabricated on the standard MED 5  $\mu\text{m}$ , 4 ohm-cm epi. This wafer had 23 good die at probe test. Wafer 21 was fabricated on 3  $\mu\text{m}$ , 18 ohm-cm Lawrence Semiconductor epi especially fabricated for low noise at temperatures below 15K. This wafer had 14 electrically good die.

The CRC 744 arrays have been thoroughly tested at SBRC, the University of Rochester, and at NASA Ames. These tests have shown very low noise and power dissipation on the 744 readout. A hybrid using an early IBC detector was loaned to NASA Ames for initial tests.

The architecture of the CRC 744 readout is shown in Figure 6.1. The active array contains 256 x 256 unit cells. The pixels are addressed by a shift register that sequentially selects each one of the 256 rows (slow scanner). At the end of each column there is a column amplifier and a multiplexer (fast scanner). The array has four outputs that read the columns in an interleaved fashion; Output 1 reads columns 1, 5, 9,... 253, Output 2 columns 2, 6, 10,... 254, Output 3 columns 3, 7, 11,... 255 and output 4, columns 4, 8, 12,... 256.

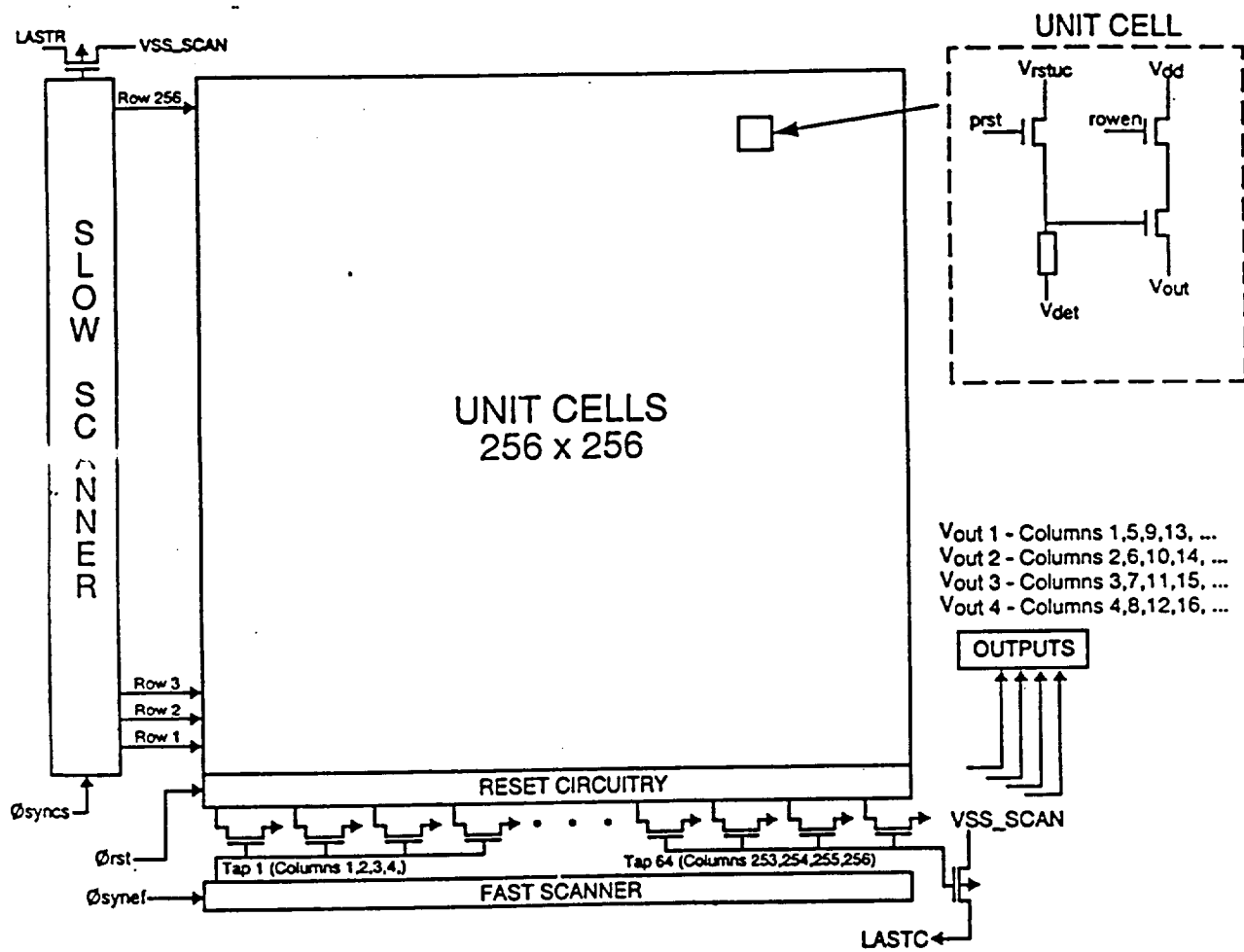


Figure 6.1 Architecture of the CRC744 readout

Figure 6.2 shows the unit cell signal path. The photocurrent from each detector is integrated onto the input capacitance. When the “rowen” switch is turned on the voltage on the input capacitance is read onto the column bus and then to the output through a buffer amplifier. The unit cells in that row and the columns are then reset.

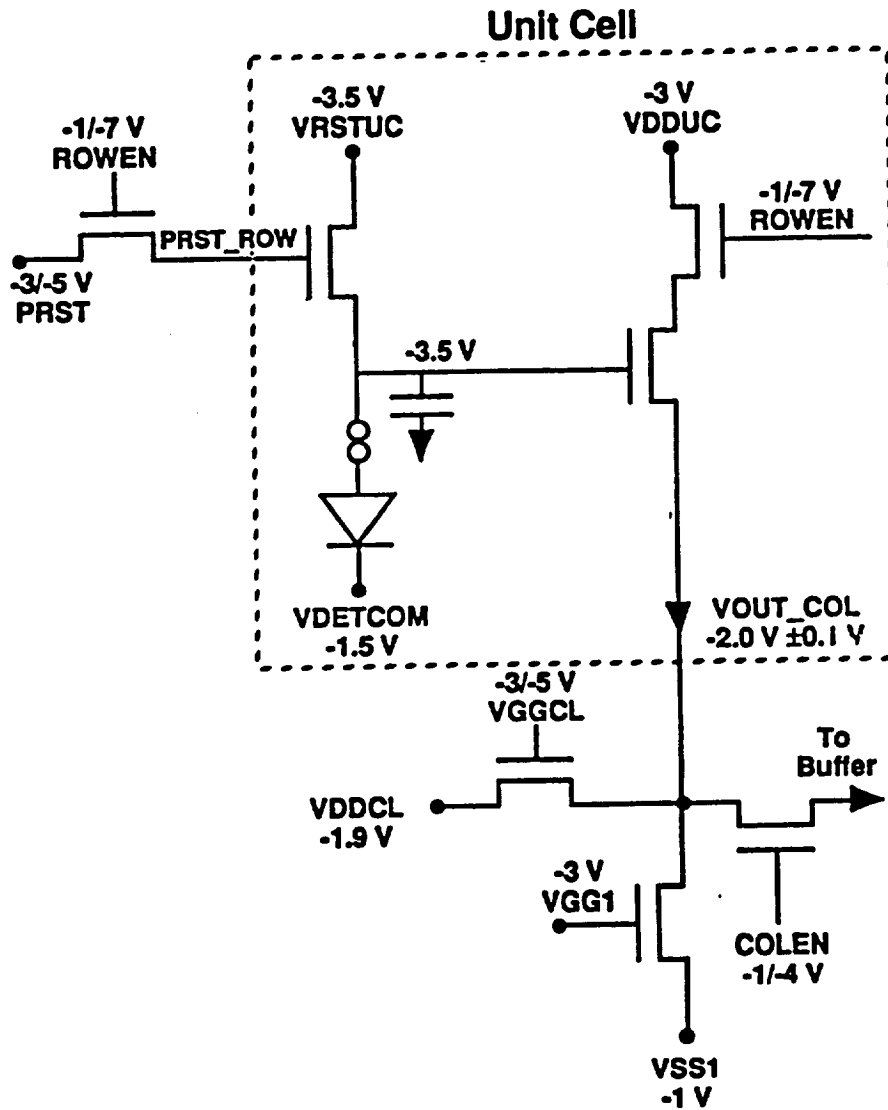


Figure 6.2 Signal path of the CRC744 readout.

## 7 SCA Fabrication

Based on the data from Table 5.1 we selected detector die from wafers 8026, 8121 and 8122. These were the three NASA wafers that had low enough residual compensation to assure full depletion. We diced the 256 x 256 region from each of the three wafers and selected two die from each wafer. These hybrids were bonded, using the bonding diagram shown in Figure 7.1 and sent to the test lab for characterization. Table 7.1 lists the assemblies and which readouts and detector wafers were used for hybridization.

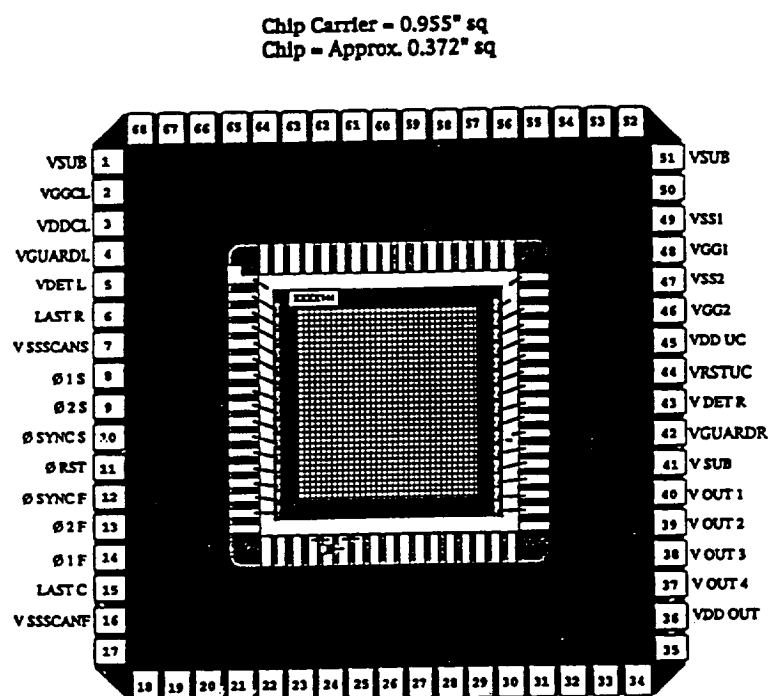


Figure 7.1 Bonding diagram of the IBC SCAs (744/778)

Table 7.1 SCA Assembly history

ASSEMBLY ID	READOUT WAFER	DETECTOR WAFER	EPI RUN
006	744-1-7-C7	8121	NASA-6 (3MS)
007	744-1-25-A5	8121	NASA-6 (3MS)
008	744-1-21-B5	8026	778-1 (3MS)
009	744-1-7-B5	8122	NASA-6 (6MS)
010	744-1-7-C2	8026	778-1 (3MS)
011	744-1-21-D7	8121	NASA-6 (6MS)

## 8 SCA Test Results

Table 8.1 lists the six SCAs tested and the main results of the tests. Each array is accompanied by a separate data pack with gray plot maps and histograms of all the parameters tested. These data was taken as a screening test to assure that the arrays were properly hybridized and the performance was acceptable for further characterization at NASA Ames with a more controlled temperature and backgrounds. For example, for the calculation of the quantum efficiency we assumed an input capacitance of 40 fF, but we have not measured it. Thus, the quantum efficiency will not be accurate if the capacitance is different from that assumed.

The uniformity and operability of all these arrays is quite high. Many arrays have all pixels working and a few have just a couple of bad pixels. These six arrays should be a perfect vehicle to understand the ultimate performance of the IBC detectors on this readout configuration.

**Table 8.1 Six SCAs Tested**

SCA ID	BIAS (V) (VOLTS)	Q.E. (%)	READ NOISE (e <sup>-</sup> )	DARK CURRENT (aA)	UNIFORMITY (STD DEV/AVE) (%)
006	0.7	56	31	3.9	7.1
007	1.5	66	44	0.56	7.5
008	1.0	38	102	?	5
009	1.25	59	27	1.9	6.7
010	1.5	40	89	4.5	5.5
011	1.0	23	27	0.28	4.5

All the SCAs had a power dissipation well below 1 milliwatt. Table 8.2 lists the biases used for Assembly 011. All the voltages for the other SCAs were the same except for the detector bias, which changed depending on what detector we were testing.

**Table 8.2 Biases and clock values used to test SCA 011. All other SCAs were tested in a very similar manner.**

**FPA# IBC-011**

<u>BIAS NAME</u>	<u>CURRENT</u>	<u>VOLTAGE</u>	<u>POWER</u>
VDDCL	-1.52E-06	-1.90	2.89E-06
VGUARD	0.00E+00	-3.00	0.00E+00
VSSSCAN	-4.70E-05	-1.00	4.70E-05
VDET	0.00E+00	-3.00	0.00E+00
VRSTUC	0.00E+00	-3.00	0.00E+00
VDDUC	-1.85E-04	-3.00	5.55E-04
VGG1	-3.94E-06	-3.00	1.18E-05
VSS1	0.00E+00	0.00	0.00E+00
VGG2	0.00E+00	0.00	0.00E+00
VSS2	0.00E+00	0.00	0.00E+00
VDDOUT	-6.17E-05	-1.20	7.40E-05
TOTAL POWER DISSIPATION=			<b>6.91E-04</b> WATTS

<u>CLOCK NAME</u>	<u>HIGH RAIL</u>	<u>LOW RAIL</u>
PHISYNC S	-1.00	-7.00
PHI 1 S	-1.00	-7.00
PHI 2 S	-1.00	-7.00
PHISYNC F	-1.00	-7.00
PHI 1 F	-1.00	-7.00
PHI 2 F	-1.00	-7.00
PHIRST	-3.00	-5.50
VGGCL	-1.00	-5.00

All SCAs had excellent operability. Figure 8.1 shows the quantum efficiency gray map of SCA 011 measured at 7.25  $\mu\text{m}$ . Even the points that look dark on the gray plot have an acceptable response, therefore, they are included in the standard deviation. None of the 65536 pixels were rejected. Many of the other arrays had similar gray plots.

## Quantum Efficiency (400K-293K), SCA #IBC

Part # CRC-744-1-21-D7	Register # 998
Serial # SCA #IBC-0118	Secondary acquisition # 10
Operator: Michael S Smith	Date acquired: 28-APR-1997 10:28:59.16
Version: VMS 5.4-3, IFPATS 1 V1.0.0	Date printed: 29-APR-1997 13:09:14.97
VRSTUC,VDDUC,VGUARD=3.0; VSSSCSAN=-1.0; VGG1=-3.0; VDDOUT=-1.2;	
Aperture: 0-1, DC flux: 3.140E+07, AC flux: 3.819E+09	
Vdet Bias: +0.500 volts	
Tint: 1.000 sec, Gain: 50.0, Frames: 10, Temp: 5K, 2DFPA Dewar	
Outputs#1 - 4	2DATA:FPA_IBC011_SIG1.REGS

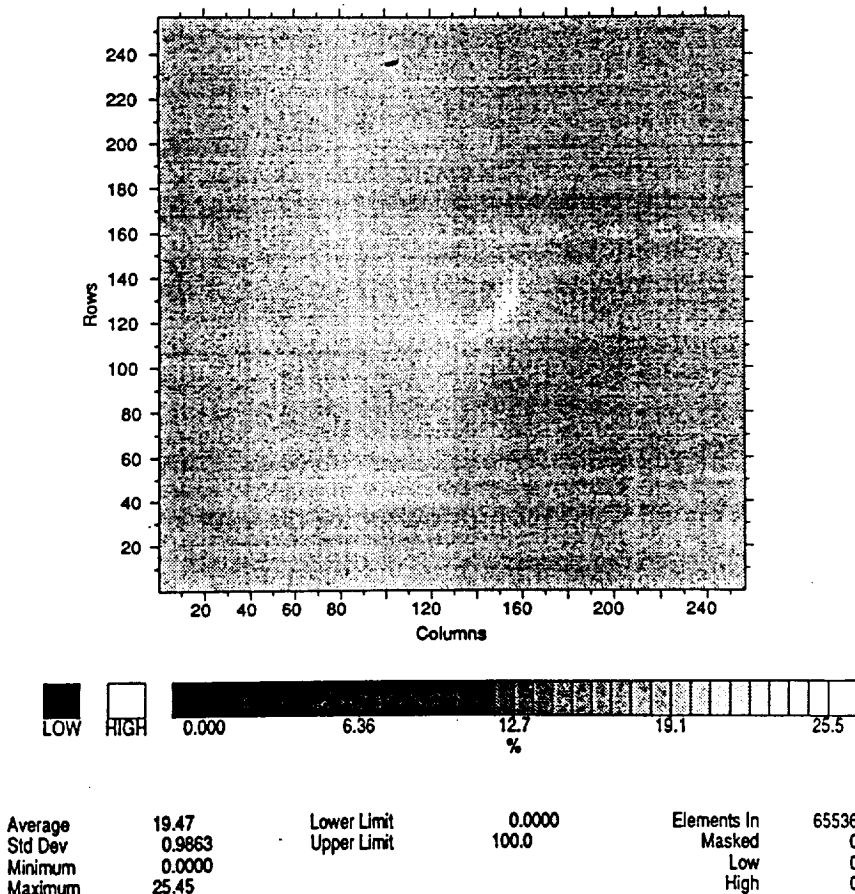


Figure 8.1 Gray plot of the quantum efficiency of SCA 011.

## 9 Conclusion

SBRC performed all the tasks stated in the Statement of Work, processing and testing more wafers and devices than initially planned. Although the program was performed at cost, the deliveries were about six months late; however, we delivered a few more parts than the program initially requested.

Technically, we were able to fabricate parts that appear to have very good performance and very low dark current. Nevertheless, because some of the epi runs yielded parts that could not be fully depleted, we were not able to have sufficient variations to fully understand the dark current mechanism.

For this program SBRC also initiated the careful testing of detectors at very low temperatures and backgrounds, something that we have not had much experience. The temperature and the background were very stressful on our testing facilities.

SBRC is now better positioned to proceed with the additional work of fabricating low dark current SCAs for ultra low backgrounds and temperatures.

SBRC fabricated on this program detectors with very low dark current and relatively high arsenic concentration. This is encouraging since we were concerned that higher arsenic concentration would lead to higher (perhaps unacceptably high) dark currents. Unfortunately we were not able to compare this performance to lower-doped detectors. Some of the other factors that we hoped to explore did not work out, simply due to the much higher than anticipated compensating impurity concentration. To deconvolve these effects will require future effort. However several noteworthy observations were achieved.

The six mask process consistently yielded dark current that dropped more rapidly with decreasing temperature than did the three mask process. This is surprising since the difference in processing primarily affects the silicon surface, which we did not believe played a significant role in the dark current. The difference in slope do not lead to huge differences in dark current at 8K, but it will be important to determine the difference at lower temperature using SCA measurements.

Processing the old epi material with the new lot for this program yielded dark currents that were not radically different from the earlier devices fabricated from wafers in the same epi run. This is encouraging since it implies stability of the process and consistency of operation on wafers fabricated from the same epi run. It also demonstrated some process robustness that makes processing only a second order effect on dark current. Again, SCA measurements at lower temperature may indicate more significant differences due to processing.

It is difficult to draw conclusions at this time on the dependence of dark current on electric field strength. The variability on compensation from run to run will require a great deal of analysis to deconvolve it from other effects. We hope to study the bias dependence of the heavily and lightly compensated detectors to infer something about the electric field effects in a future program.

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